Yuntao Lu

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Research Interests

- Machine Learning in Electronic Design Automation (EDA), especially, power prediction & optimization, and functional verification.

Experience

Jan. 2022 – Aug. 2023, Shanghai, China
- **Intel Asia-Pacific Research & Development Ltd**
  Machine Learning Engineer, Artificial Intelligence & Analysis Group
  • Projects: Validations for Intel TensorFlow, and Intel oneAPI AI Analytics Toolkit

Aug. 2018 – May 2020, Beijing, China
- **The Institute of Computing Technology, Chinese Academy of Sciences**
  AI Applied Engineer, Intelligent Processor Research Center
  • Projects: Validations and Developments for Optimized AI models and applications on AI-specific chips.

Education

Aug. 2023 – At present, Hong Kong, China
- **The Chinese University of Hong Kong**
  Ph.D. Candidate, Department of Computer Science and Engineering

Aug. 2018 – May 2020, Austin, Texas, U.S.
- **The University of Texas at Austin**
  M.S., School of Information

Sep. 2015 – Jun. 2018, Hefei, Anhui, China
- **University of Science and Technology of China**
  M.S., School of Computer Science and Technology

Sep. 2011 – Jun. 2015, Chengdu, Sichuan, China
- **University of Electronic Science and Technology of China**
  B.Eng, School of Information and Software Engineering

Publications

Journal Papers

1. **Yuntao Lu**, Chen Bai, Yuxuan Zhao, Ziyue Zheng, Yangdi Lyu, Mingyu Liu, and Bei Yu, "DeepVerifier: Learning to Update Test Sequences for Coverage-Guided Verification," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 2025.
2. **Yuntao Lu**, Chao Wang, Lei Gong, and Xuehai Zhou, "SparseNN: A Performance-efficient Accelerator for Large-scale Sparse Neural Networks," *International Journal of Parallel Programming (IJPP)*, vol. 46, no. 4, pp. 648–659, 2018.

Conference Papers

1. **Yuntao Lu**, Dehua Liang, Siting Liu, Yuhao Ji, Yu Zhang, Xuanqi Chen, Xia Lin, Jinlei Lu, *et al.*, "A Hybrid Optimization Framework for Power-Efficient Pulsed Latch Utilization in Clock Networks," in *ACM/IEEE Workshop on Machine Learning CAD (MLCAD)*, 2025, pp. 1–8.

2 **Yuntao Lu**, Mingjun Wang, Yihan Wen, Boyu Han, Jianan Mu, Huawei Li, and Bei Yu, "VIRTUAL: Vector-based Dynamic Power Estimation via Decoupled Multi-Modality Learning," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2025, pp. 1–9.

3 Yuhao Ji, **Yuntao Lu**, Zuodong Zhang, Zizheng Guo, Yibo Lin, and Bei Yu, "DiffCCD: Differentiable Concurrent Clock and Data Optimization," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2025, pp. 1–9.

4 **Yuntao Lu**, Lei Gong, Chongchong Xu, Fan Sun, Yiwei Zhang, Chao Wang, and Xuehai Zhou, "A High-performance FPGA Accelerator for Sparse Neural Networks: Work-in-progress," in *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, 2017, pp. 1–2.

5 Chongchong Xu, Jinhong Zhou, **Yuntao Lu**, Fan Sun, Lei Gong, Chao Wang, Xi Li, and Xuehai Zhou, "Evaluation and Trade-offs of Graph Processing for Cloud Services," in *IEEE International Conference on Web Services (ICWS)*, 2017, pp. 420–427.

Book Chapters

1 **Yuntao Lu**, Chao Wang, Lei Gong, Xi Li, Aili Wang, and Xuehai Zhou, "Overview of Neural Network Accelerators," in *High Performance Computing for Big Data*, Chapman and Hall/CRC, 2017, pp. 107–120.